RESPONSE under 37 C.F.R. § 1.111
U.S. Appln. No. 10/027,978

AMENEMENTS TO THE CLAIMS:

Claims 1.-13. (Cancelled)

14. (Currently amended) An apparatus, comprising:

a memory controller; and

a table walk device connected to the memory controller and externally located from a memory management unit (MMU).

15. (Previously presented) The apparatus of claim 14, wherein the table walk device combines a portion of a virtual address and a portion of a base address.

16. (Previously presented) The apparatus of claim 14, wherein the table walk device comprises a table base register to store a table base address.

17. (Previously presented) The apparatus of claim 14, further comprising a translation lookaside buffer (TLB) coupled to the table walk device.

18. (Previously presented) The apparatus of claim 17, wherein the table walk device generates a descriptor and the TLB is adapted to receive the descriptor from the table walk device.

19. (Previously presented) The apparatus of claim 14, wherein the table walk device is adapted to receive memory access protection data.

20. (Previously presented) The apparatus of claim 14, wherein the apparatus further comprises:

a processor coupled to the table walk device; and

a memory device coupled to the memory controller.

21. (Previously presented) The apparatus of claim 20, wherein the table walk device is adapted to determine whether a process executing in the processor is permitted to access data stored in the memory device.

22. (Previously presented) The apparatus of claim 21, wherein the table walk device transmits an abort signal to the processor if the process is not permitted to access data stored in the memory device.

23. (Previously presented) A system, comprising:

a processor;

a discrete memory controller adapted to perform a table walk operation and coupled to the processor; and

a volatile memory device coupled to the discrete memory controller.

24. (Previously presented) The system of claim 23, further comprising a memory management unit (MMU), wherein the discrete memory controller is coupled to the processor via the MMU.

25. (Previously presented) The system of claim 24, wherein the MMU is adapted to provide memory access protection by preventing a process executing in the processor from accessing predetermined data in the volatile memory device.

26. (Previously presented) The system of claim 23, wherein the discrete memory controller is adapted to provide address translation by using results of the table walk.

27. (Previously presented) The system of claim 23, wherein the discrete memory controller performs a table walk by combining a portion of a virtual address and a portion of a base address to generate an address of a descriptor.

28. (Previously presented) The system of claim 23, wherein the volatile memory device is a dynamic random access memory (DRAM) device.

Claims 29.-33. (Cancelled)